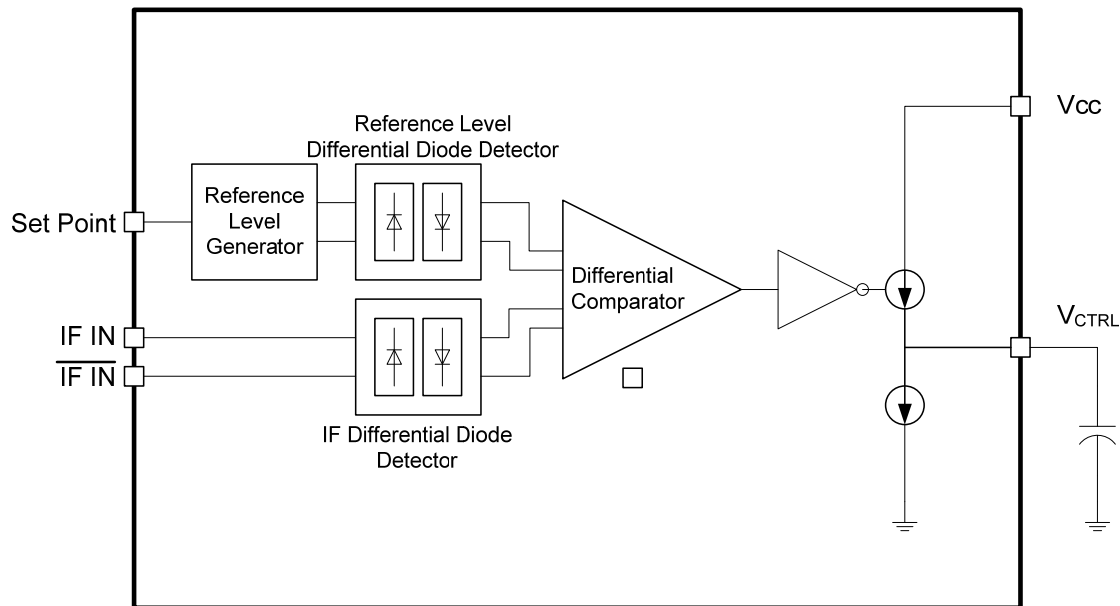


Block Diagram



Typical Applications

- GPS Receivers
- Galileo Receivers
- GLONASS Receivers
- L1 and L2 Dual Band Receivers
- General Purpose AGC

Key Features

- User Programmable Response Time
 - ❖ 10 μ s with 100pF Capacitor
 - ❖ 400ms with 1 μ F Capacitor
- Self Contained, No Processor Required
- Compatible with TRFS30005 AGC amplifier

IP Block Overview

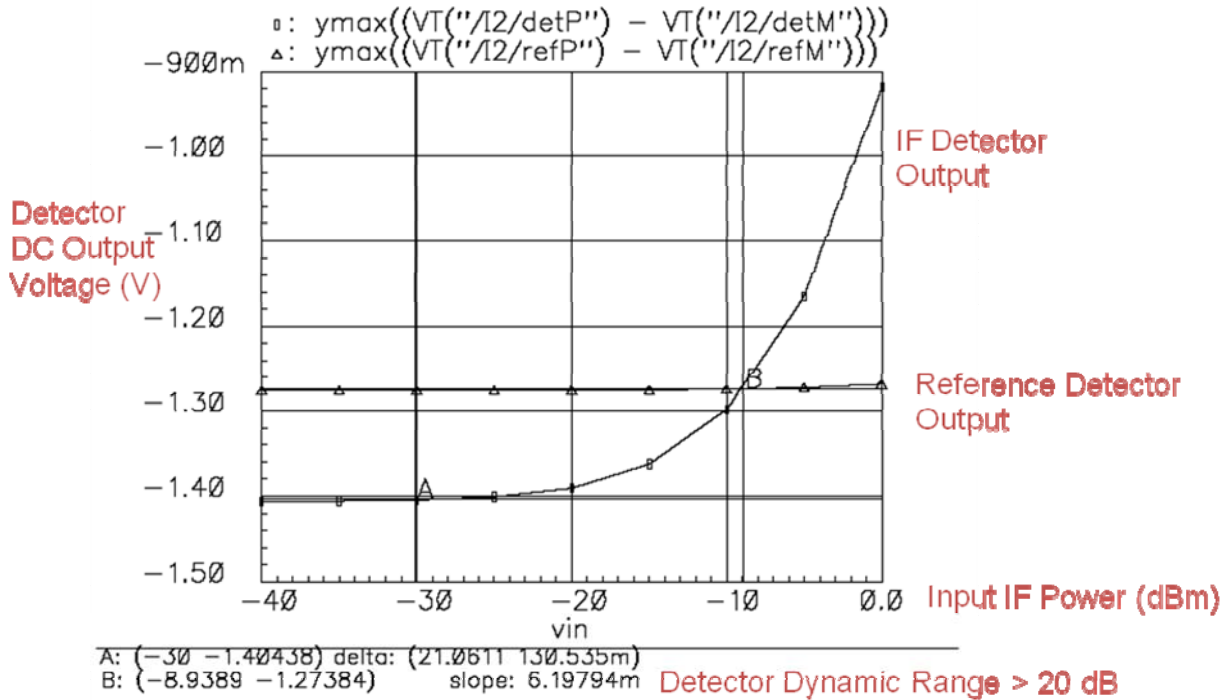
The TRFS06001 IP is an IF level detector/AGC circuit. It is designed to maintain a constant IF signal peak to peak voltage. Typically this voltage is set to 0.5V. The detector and AGC loop is comprised of two differential diode detectors, a comparator and current sources to charge or discharge the external decay/attack rate capacitor. The IF signal is fed into a diode detector. This rectified signal is compared to a rectified reference. The comparison output controls a current that charges up the

external capacitor. Using an external capacitor allows user control of the decay/attack rate. A wide range of capacitors can be used to vary the attack/decay time from microseconds to milliseconds.

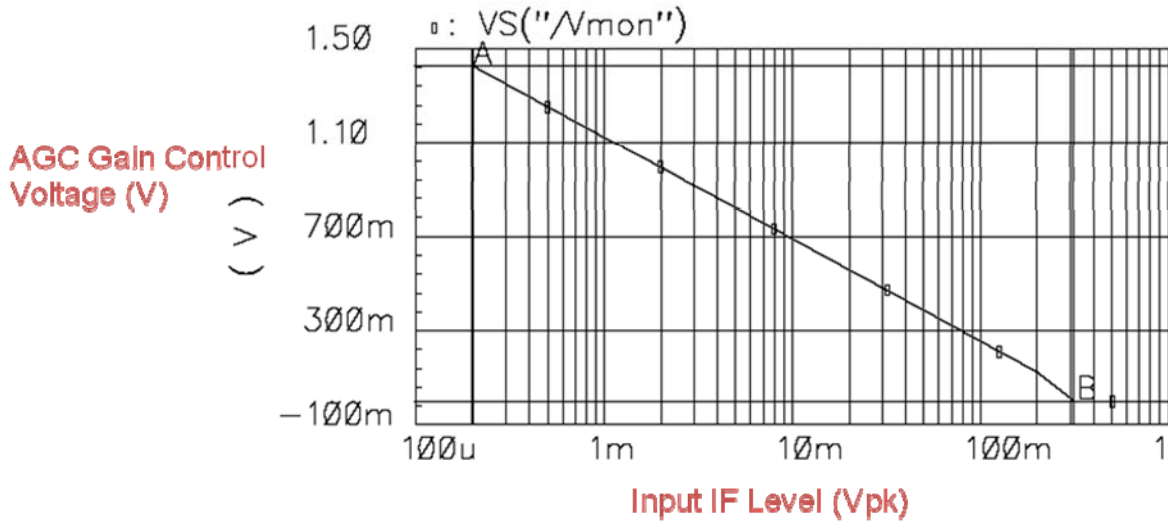
IP Block Performance Summary

Specification	Conditions	MIN	TYP	MAX	Units
Temperature Range		-40	25	85	°C
V _{BAT}		2.7	2.85	3.0	V
Detected Signal Level			0.5		V _{p-p}
Dynamic Range					
AGC Response Time	Set with external capacitor (100pF to 1μF)	0.01		400	ms

Detector Voltage vs. 175 MHz IF Signal Input



AGC Gain Set Voltage vs VGA Input Voltage



The dynamic range of gain control is 65 dB when using the detector with a 65 dB IF variable gain amplifier.

Known Limitations/Issues

Revision History

Revision #	Date	Notes
V1.0	07-Jan-2009	Initial Draft
V1.1	13-Jan-2009	Added plots
V1.2	14-Jan-2009	Initial Customer Release