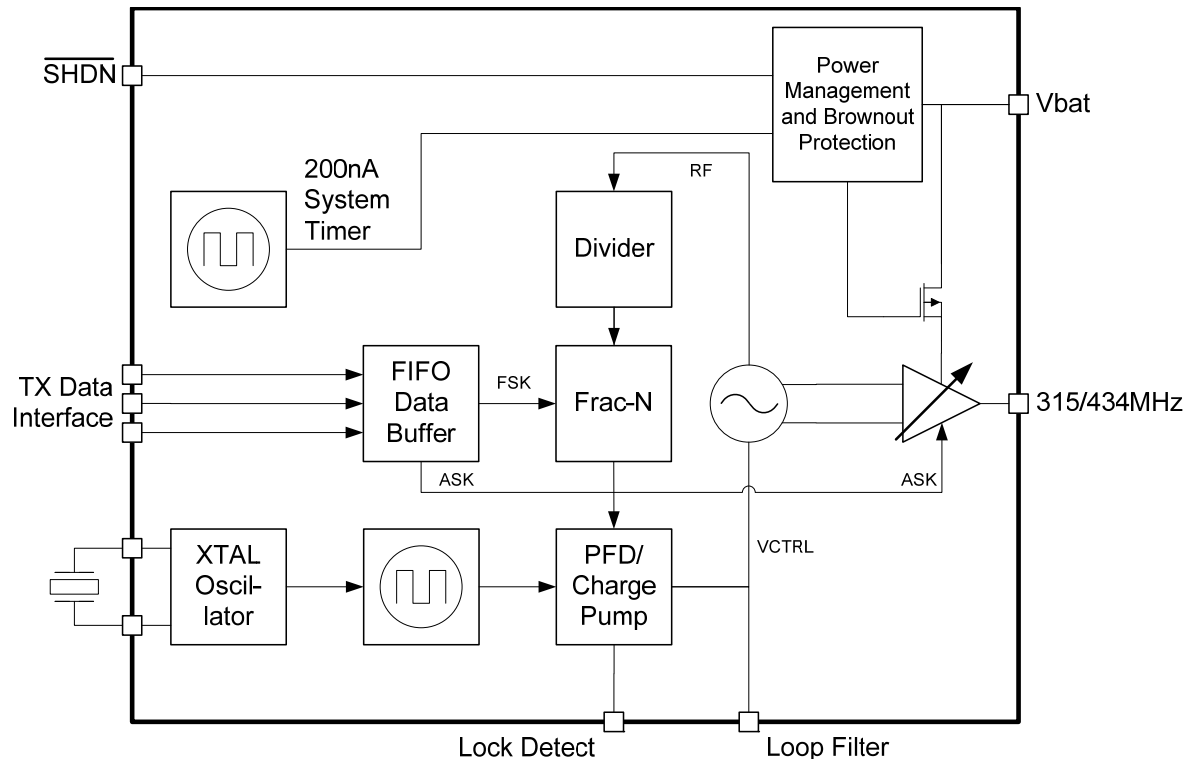


Block Diagram



Typical Applications

- Remote Keyless Entry Transmitters
- Home Automation
- Wireless Telemetry
- Integration with Microcontroller

Key Features

- 250nA System Wake-Up Timer requires no External Components
- XTAL- based TX Architecture has excellent Frequency Stability
- Supports both ASK and FSK modulation
- Software programmable RF (315/434MHz)
- Low Cost Automotive Qualified CMOS process
- Programmable Output Power from +8dBm to -2dBm
- <15mA @ +8dBm output power

IP Block Overview

The TRFS25007 IP has been designed for lowest current consumption and low cost. It includes an ultra low power system timer (250nA) that does not require any external components. In a typical application, this timer can eliminate the space and cost associated with a 32KHz clock crystal. The transmitter section's carrier frequency is generated using a PLL synthesizer using on chip crystal oscillator circuitry stabilized by an off-chip crystal. The transmit data is stored in an on-chip FIFO buffer and can be programmed to be transmitted using either ASK or FSK modulation. The carrier frequency can be electronically controlled between 315MHz and 434MHz. The transmit signal can be used to directly drive an antenna without the need of external SAW filtering. A system power management block allows the selection of various power modes, from complete sleep (<1uA) to full power transmit (13mA) and various modes in between. The transmit power is programmable in 1dB steps from +8dBm to -2dBm to allow for an optimum range/current consumption trade-off. This IP has been implemented on a low cost CMOS process. Integration of this IP block with other analog and digital circuitry has been demonstrated.

IP Block Performance Summary

Specification	Conditions	MIN	TYP	MAX	Units
Temperature Range		-40	25	100	°C
V _{BAT}		1.8		3.6	V
Supply Current	Only system timer on		0.2		μA
	VCO locked (pre-TX)		3		mA
	Full transmit (0dBm)		6		mA
	Full transmit (+8dBm, V _{cc} =3.0V)		12		mA
Output Frequency	Band=High		315		MHz
	Band-Low		434		
FSK Modulation Baud Rate		1		100	kHz
ASK Modulation Baud Rate		1		20	kHz

Specification	Conditions	MIN	TYP	MAX	Units
ASK on/off ratio		40			dB
PLL Startup Time	Using appropriate loop filter			2	ms
PLL Lock Detect Accuracy	Deviation from programmed value			0.01	%
VCO phase noise	@1MHz offset		-100		dBc/Hz
Output spurious	Fundamental < f < 2 nd Harmonic			40	dBc
Output Power	Vcc=3.0V, Highest Setting		8		dBm
	Vcc=1.8V Highest Setting	-1			
Output Power Steps	0.5dB < Step Size < 2dB		10		

Known Limitations/Issues

Revision History

Revision #	Date	Notes
V1.0	19-Dec-2008	Initial Draft
V1.1	12-Jan-2009	Updated data interface, corrected numbers in features
V1.2	14-Jan-2009	Initial Release